## AMENDMENTS TO THE CLAIMS

1-18. (cancelled)

19.(currently amended) A ~~nonvolatile memory~~Mask ROM, comprising:
a substrate having source/drain formed at unselected side and source/drain with extension source/drain formed at other selected side, wherein a "digital zero" area is defined in said source/drain formed at said unselected side, and "digital one" area is defined in said source/drain with extension source/drain;
gate dielectric layer formed on said substrate;
gate formed on said gate dielectric layer;
isolation layer formed along the surface of said gate; and
spacers formed attached on the sidewalls of said isolation layer.

20.(currently amended) The ~~nonvolatile memory~~Mask ROM of Claim 19, wherein the thickness of said gate is approximately 800-2500 angstroms.

21.(currently amended) The ~~nonvolatile memory~~Mask ROM of Claim 19, wherein the thickness of said gate dielectric layer is approximately 10-250 angstroms.

22.(currently amended) The ~~nonvolatile memory~~Mask ROM of Claim 19, wherein the thickness of said isolation layer is approximately 20-200 angstroms.

23.(currently amended) The ~~nonvolatile memory~~Mask ROM of Claim 19, wherein the width of said spacer are approximately 200-2000 angstroms.

24.(currently amended) The ~~nonvolatile memory~~Mask ROM of Claim 19, further comprising silicide on said gate~~, first~~ and source/drain regions.

25.(currently amended) The ~~nonvolatile memory~~Mask ROM of Claim 19, wherein said

gate dielectric layer includes oxide or the material with high dielectric constant.

26.(currently amended) The ~~nonvolatile memory~~Mask ROM of Claim 25, wherein said dielectric constant of said high dielectric constant is around 3-100.

27.(currently amended) The ~~nonvolatile memory~~Mask ROM of Claim 26, wherein said material with high-k (dielectric constant) is selected from $Ta_2O_5$, $Al_2O_3$, $ZrO_2$, $HfO_2$, $Gd_2O_3$ or $Y_2O_3$.

28.(currently amended) The ~~nonvolatile memory~~Mask ROM of Claim 19, wherein said spacers are formed of the material selected form oxide, nitride or the combination thereof.

29.(currently amended) The ~~nonvolatile memory~~Mask ROM of Claim 19, wherein the ion source for said source/drain is selected from the group consisting of phosphorus, arsenic, boron and the combination thereof.

30.(currently amended) The ~~nonvolatile memory~~Mask ROM of Claim 19, further comprising a pocket ion implantation region formed adjacent to said gate or source/drain, wherein the conductive type of said pocket ion implantation region is opposite to the one of said source/drain.

31-34.(cancelled)

## AMENDMENTS TO THE SPECIFICATION

Please amend paragraph [0018] as follows:

"FIGURE 1a-1c are cross sectional views of semiconductor wafer illustrating the example according to the prior art~~present invention~~."

Please amend the Abstract as follows:

"The structure of the nonvolatile memory ~~comprises~~ includes a substrate having source/drain formed at unselected sides and source/drain with extension source/drain formed at other selected sides. A gate dielectric layer is formed on the substrate and a gate is formed on the gate dielectric layer. An isolation layer is formed along the surface of the gate. Spacers are formed attached on the sidewalls of the gate."